TECHNICAL NOTE 168

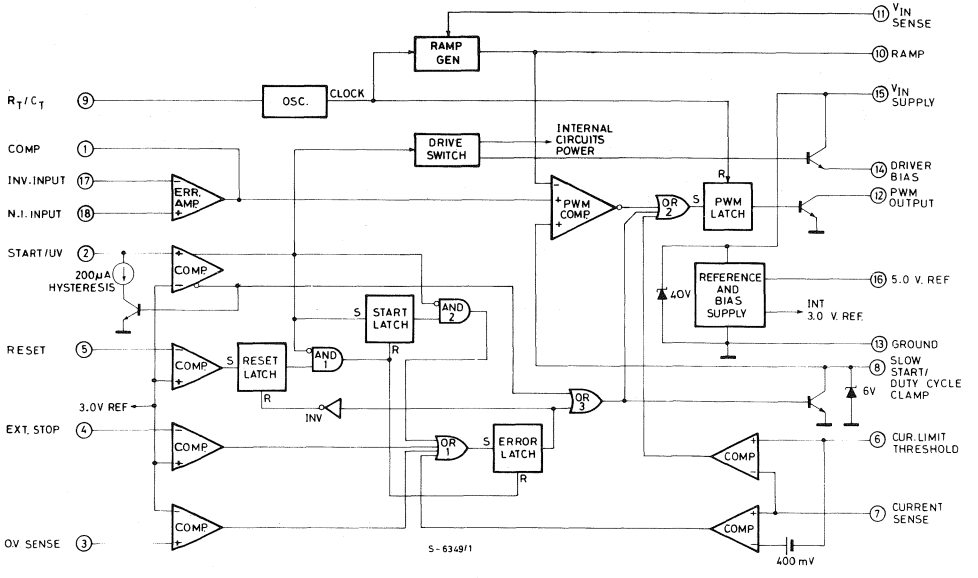
APPLYING THE UC1840 TO PROVIDE TOTAL CONTROL FOR LOW-COST, PRIMARY-REFERENCED SWITCHING POWER SYSTEMS

INTRODUCTION

There are many potential approaches to be considered in switch mode power supply design; however, the contradictory requirements of minimum cost and compatibility with ever more demanding line isolation specifications make primary control very attractive. Application of the UC1840 as a primary-side, off-line controller presents an extremely cost-effective approach to supplying isolated power from a widely varying input line while maintaining a high degree of efficiency.

Primary control means referencing all of the control electronics along with the power switching device on the input line side of an isolation transformer. An obvious advantage to this approach is the simplified interface between the control and

Fig. 1 - The overall block diagram of the UC1840, an integrated circuit optimized for primary-side control of off-line switching power supplies.



power switch. This eliminates many of the transitions across the isolation boundary which significantly increase the cost of the magnetics portion of the power supply's budget.

There are two disadvantages to primary control: (1) operating or at least starting, the control electronics from the line voltage (typically 300 VDC), and (2) providing adequate regulation (which requires feedback from the secondary across the isolation boundary). The capability of the UC1840 Control IC to solve these problems while providing all of the regulating, sequencing, monitoring, and protection functions referenced to the primary side, makes this device very attractive.

THE UC1840 CONTROLLER

The overall block diagram of the UC1840, shown in Figure 1, includes the following features:

(1) Fixed-frequency operation set by user-selected components.

(2) A variable-slope ramp generator for constant volt-second operation providing open-loop line regulation and minimizing, or in some cases even eliminating, the need for feedback control.

(3) A drive switch for low current start-up off the high-voltage line.

(4) A precision reference generator with internal over-voltage protection.

(5) Complete under-voltage, over-voltage, and over-current protection including programmable shutdown and restart.

(6) A high-current, single-ended PWM output optimized for fast turn-off of an external power switch.

(7) Logic control for pulse-commandable or DC power sequencing.

For an understanding of how these individual blocks work together in a typical, medium-power flyback power supply, reference should be made to Figure 2 and the functional description which follows.

UC1840 FUNCTIONAL DESCRIPTION

Power sequencing

A simplified schematic of the UC1840's internal power turn-on circuitry is shown in Figure 3. The key elements of this function are: (1) the Driver Bias Switch, Q3, which keeps the loading on the control voltage line, V_C, to a minimum during start up; (2) the Under-voltage Comparator which also functions as a Start Threshold Detector with programmable hysteresis; and (3) an auxiliary, primary-referenced, low-voltage winding on the main power transformer which provides normal control power after turn-on. The sequence of events is as follows:

Fig. 2 - A fully protected, isolated flyback power supply can be implemented with the UC1840, a high-voltage power switch, the transformer, and a small handful of passive components.

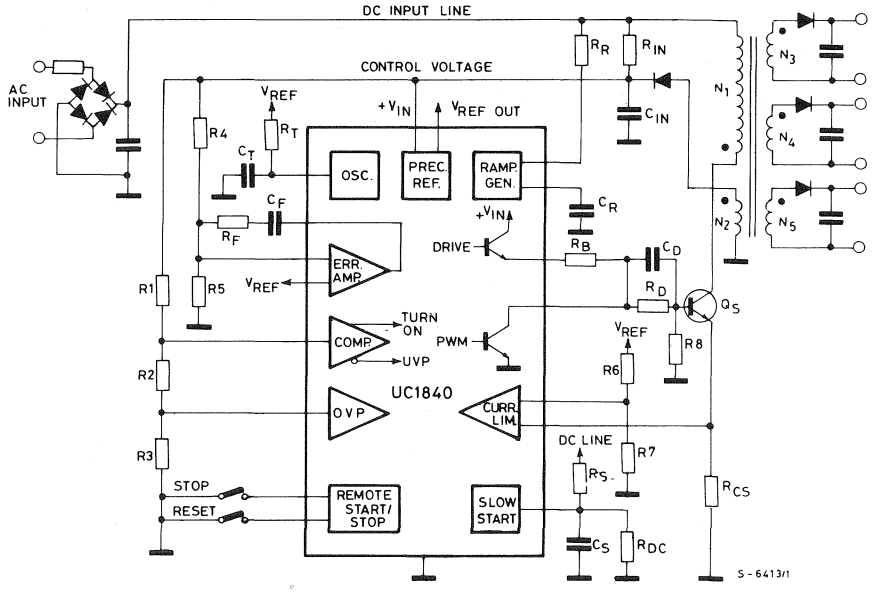
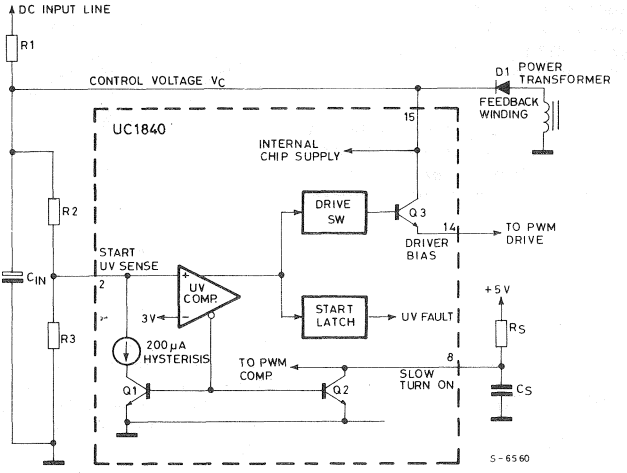


Fig. 3 - The UC1840's start circuitry requires low starting current from the DC input line with normal operating current supplied from a low-voltage feedback winding on the power transformer.



(1) While the control voltage, V_C, is low enough so that the voltage on pin 2 is less than 3V, the Start/UV Comparator does the following:

(a) A 200μA hysteresis current is flowing into pin 2 through Q1 causing an added drop across R2.

(b) The drive switch is holding the Driver Bias transistor, Q3, OFF. This insures that the only current required through R1 is the start-up current of the UC1840, plus external dividers (R2, R3, R_S, etc.).

(c) The Slow Turn-on transistor, Q2, is ON, holding pin 8 and C_S low.

(d) The Start Latch keeps the under-voltage signal from being defined as a fault.

(2) The start level is defined by:

$$V_C \text{ (start)} = 3 \left(\frac{R2 + R3}{R3}\right) + 0.2\ R2.$$

When V_C rises to this level, the Start/UV. Comparator then does the following:

(a) Turns off Q1, eliminating the 200μA hysteresis current. This allows the voltage on V_C to drop before reaching the under-voltage fault level defined by:

$$V_C \text{ (U.V. fault)} = 3 \left(\frac{R2 + R3}{R3}\right)$$

(b) Sets the Start Latch to monitor for an under-voltage fault.

(c) Activates Q3 providing Driver Bias to the power switch, pulling the added current out of C_{IN}.

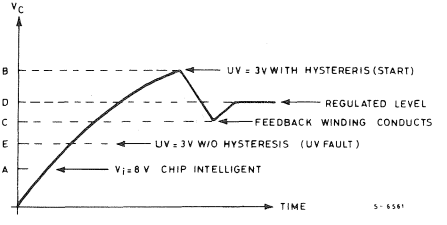
(d) Turns off Q2 allowing for programmed slow turn-on defined by R_S and C_S.

(3) A normal start-up occurs with the control voltage, V_C, following the path shown in Figure 4. If the power supply does not start, V_C will fall to an under-voltage fault which will then either initiate a restart attempt or hold the power switch off, depending upon the status of the Reset terminal as defined under Fault Sequencing. If start-up does not occur because of some fault in the Driver Bias line, V_C will continue to rise until the 40V zener across the reference circuit conducts. This will then clamp V_C to that level, protecting the control chip.

After start-up occurs, current will continue to flow in R1 providing a power loss of:

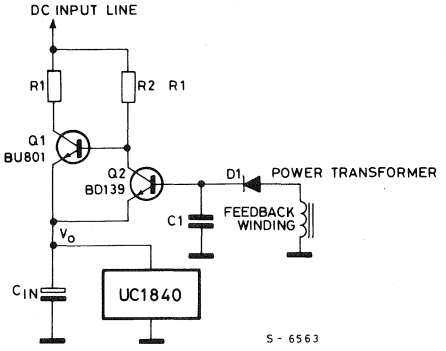
$$Pd = \frac{(V_{line} - V_C)^2}{R1}$$

Fig. 4 - Under a normal turn-on, the supply voltage to the UC1840, V_C, would rise lightly loaded to the start level, fall under the turn-on load, and then regulate at some intermediate level.



If this loss is objectionable, it can be reduced more than an order of magnitude by the addition of a two-transistor switch shown in Figure 5. In this circuit, Q1 is initially driven on by current through R2. When the feedback winding starts to conduct through D1, however, Q2 turns on leaving only R2 conducting from the input line.

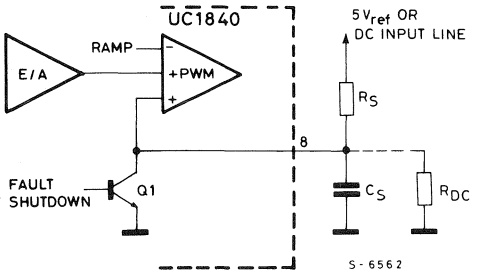
Fig. 5 - The addition of Q1 and Q2 can eliminate the steady-state current through R1 after turn-on. Q2 is selected to pass all control current through its base-emitter junction.



Slow turn-on circuit

The PWM comparator input connected to pin 8 accommodates several programming functions, shown in Figure 6. Since this comparator will only follow the lowest positive input, holding pin 8 low will effectively eliminate a PWM signal, regardless of the status of the Error Amplifier output. Prior to turn-on, and at all times when a fault has been sensed, Q1 is ON, holding pin 8 low.

Fig. 6 - Pin 8 on the UC1840 can be used for both slow turn-on and duty-cycle limiting as well as a PWM shutdown port.

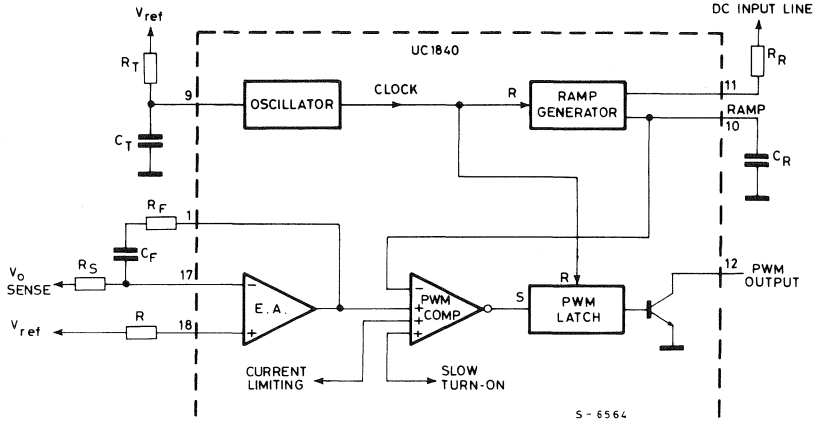


When Q1 turns off, allowing pin 8 to rise with a controlled rate will cause the output pulses to increase from zero to nominal widths at the same rate. This is accomplished by the addition of C_S and a charging source, such as R_S, to the 5V reference.

Note that where starting energy is stored in an input capacitor, the time for PWM turn-on must be less than the time required for the added Driver Bias load current to discharge the input capacitor to the under-voltage fault level. In other words, referring back to Figure 4, the slow turn-on must be faster than the time required for V_C to fall from level B to level E.

Another function of pin 8 is to establish a maximum duty cycle limit. This is achieved by clamping the voltage on pin 8 with a divider formed by adding R_{DC} to ground. If R_S is taken to the 5V reference, the clamp voltage will be fixed, which is desirable if the ramp slope is also fixed. If the ramp slope is varied with the input line — for constant volt-second operation — then the clamp voltage on pin 8 must also vary. This is readily accomplished

Fig. 7 - The pulse-width modulator within the UC1840 separates the ramp function from the fixed-frequency oscillator.



by connecting R_S to the DC input line. The divider voltage:

$$V_{Pin\ 8} = \left(\frac{R_{DC}}{R_S + R_{DC}}\right) V\ DC\ input$$

should be equal to the ramp voltage level that yields the desired maximum duty cycle, at the same DC input level.

PWM control

Pulse-Width Modulation within the UC1840 consists of the blocks shown in Figure 7. This architecture, with the possible exception of the separation between the time-base and ramp functions, is fairly conventional. It is described in greater detail in the paragraphs which follow.

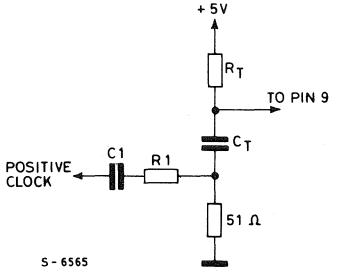
Oscillator

A constant clock frequency is established by connecting R_T from pin 9 to the 5V reference and C_T from pin 9 to ground. The frequency is approximated by:

$$f \approx \frac{1}{R_T\ C_T}$$

where the value of R_T can range from 1 kΩ to 100KΩ and C_T from 300pF to 0.1μF. The best temperature coefficients occur with C_T in the range of 1000 to 3000 pF. Although the clock output pulse is not available external to the UC1840, synchronization to an external clock can still be accomplished with the circuit of Figure 8, where R1 and C1 are selected to provide a 0.5V, 200 ns pulse across the 51Ω resistor, and R_T and C_T define a frequency slightly lower than the synchronizing source.

Fig. 8 - Synchronization to an external time base can be accomplished by adding a 51Ω resistor in series with C_T.

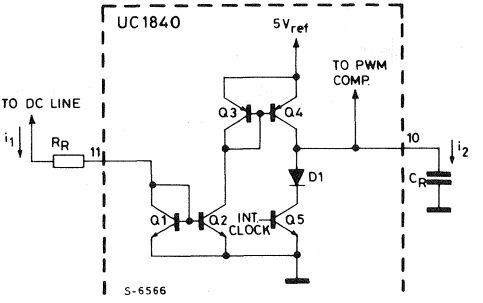


To achieve minimum start-up current, the oscillator is not activated until the input voltage is high enough to give a start command to the drive switch.

Ramp generator

The ramp generator function of the UC1840 is shown in simplified form in Figure 9.

Fig. 9 - Current mirrors Q1-Q4 are used to make the ramp charging current i_2, linearly proportional to the DC input line.



The NPN and PNP current mirrors provide a charging current to C_R of:

$$i_2 = i_1 = \frac{V_{line} - 0.7V}{R_R} \cong \frac{V_{line}}{R_R}$$

The current mirrors are useful over a current range of 1μA to 1mA, but optimum tracking occurs between 30μA and 300μA. Since the voltage across Q1 is very small, i_2 accurately represents the input line voltage. The ramp slope, therefore, is:

$$\frac{dv}{dt} = \frac{V_{line}}{R_R\ C_R}$$

The peak voltage across C_R is clamped to approximately 4.2V while the valley, or low voltage, is determined by the on-voltage of the discharge network, D1 and Q5. This is typically 0.7V.

If line sensing is not required, R_R should be connected to the 5V reference for constant ramp slope.

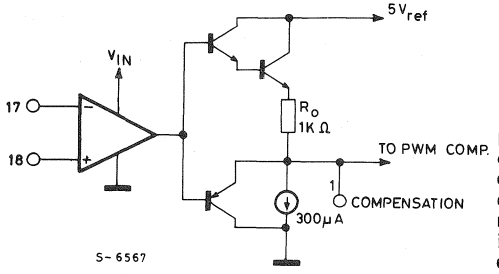
Error amplifier

This is a voltage-mode operational amplifier with an uncommitted NPN differential input stage and an output configuration as shown in Figure 10.

The 1KΩ output resistor, R_o, is used both for short circuit protection and to limit the peak output voltage to less than 4.0V so it cannot rise above the clamped ramp waveform. At sink currents less than 300 μA, the low output level will be within 200mV of ground but it rises to 1V at higher current levels.

The input common mode range is from 1V to within 2V of the input supply voltage. V_{in}, and thus either input can be connected directly to the 5V reference.

Fig. 10 - The output of the error amplifier operates class A to 300μA, but can source and sink more than 1 mA for fast response.

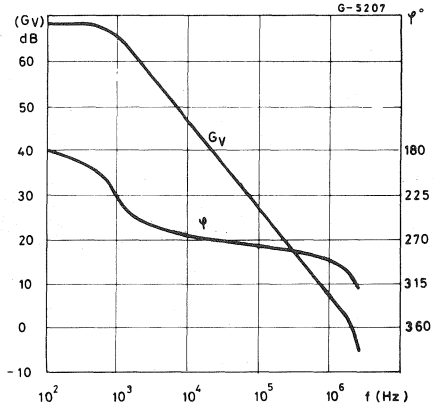


The small signal, open-loop gain characteristics are shown in Figure 11. The amplifier is unity-gain stable and has a maximum slew rate of just under 1V/μs.

PWM comparator and latch

This comparator (see Figure 7) generates the output pulse which starts at the termination of the clock pulse and ends when the ramp waveform crosses the lowest of the three positive inputs. The clock forms a blanking pulse which keeps, the maximum duty cycle less than 100%. The PWM latch insures there will be only one pulse per period and eliminates oscillation at comparator cross-over.

Fig. 11 - The UC1840 error amplifier has a DC gain of 67 dB, a 2 MHz bandwidth, and phase margin of approximately 45°.



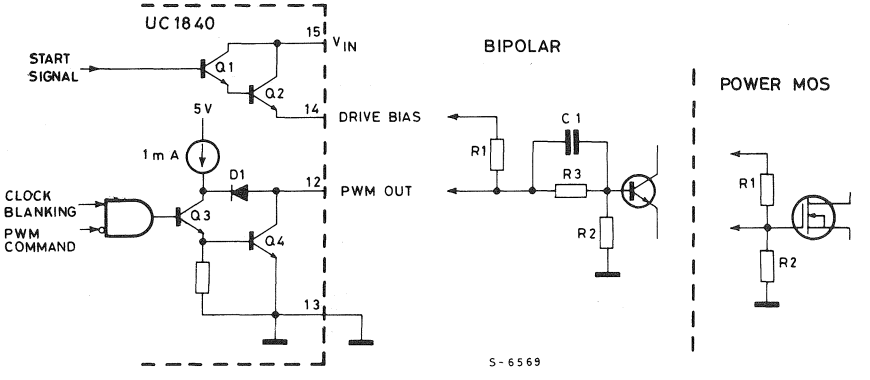
PWM output stage

In addition to the PWM output signal on pin 12, the UC1840 also includes an output gating, or arming function as Driver Bias on pin 14. Both functions should be considered together in interfacing to the external high-voltage power switch. These are illustrated in simplified form in Figure 12.

At very low input voltages (V_{IN} < 3V), both Q2 and Q4 are OFF. This may necessitate the use of R2, but its value can be high since it does not have to turn the output switch off. It merely holds it in the off state during the early portion of start-up.

Between V_{IN} = 3V and the start threshold (pin 2 = 3V with hysteresis on), Q2 is OFF and Q4 is ON, clamping the power switch off with a low impedance. A start command (UV high) turns on Q2, applying (V_{IN} - 2V) to R1. This provides a source for power switch activation; however, since Q4 is still conducting, the current through R1 is shunted to ground and the power switch remains held off.

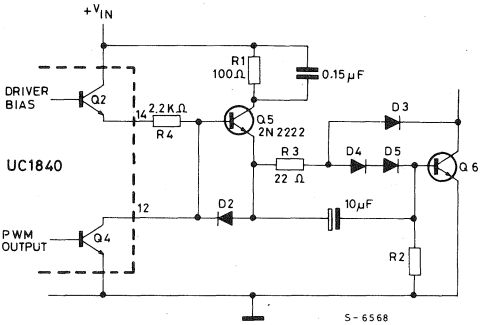
Fig. 12 - Interfacing the UC1840 PWM output stage to either Bipolar or Power MOS switches.



At the same time Q2 turns on, the clamping transistor at the slow-start terminal, pin 8, turns off allowing the voltage on pin 8 to rise according to the external slow-start time constant described earlier. This allows PWM pulses to begin to activate Q4 – narrow at first and widening to the point where the error amplifier takes command.

The interface between the UC1840 and the primary power switch may be implemented in several different ways to meet varying system requirements. One obvious application is when the use of a bipolar transistor switch requires more drive current than the Driver Bias output can provide. Figure 13 shows a more typical bipolar drive scheme where Q5 has been added to boost the turn-on current with the UC1840 still providing the high speed turn-off. The circuit now serves as a more efficient "totem-pole" driver since Q5 turns off when Q4 conducts. It also illustrates the use of a Baker Clamp to minimize storage time in Q6 and the capacitors for rapid turn-on and high-current pulse turn-off.

Fig. 13 - Adding Q5 as a switched, drive-boost transistor provides added base drive for Q6 while reducing the steady-state current through both Q2 and Q4.

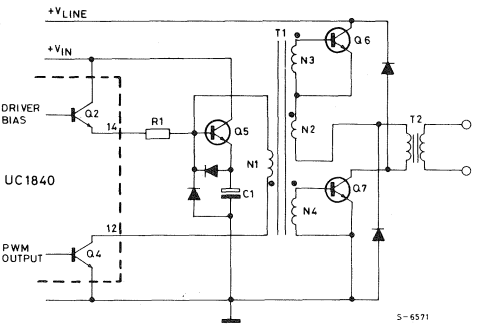


Another application is the two-transistor, off-line, forward converter topology shown in Figure 14. This circuit uses proportional base drive where the UC1840 need only supply a short, turn-off current pulse with transformer regeneration through T1 providing the steady-state drive. The magnetizing current is controlled by R1, with Q5 added to rapidly recharge C1 from which the turn-off current is supplied.

Fault protection

A significant benefit in using the UC1840 is the multi-faceted fault-sensing and programming capability built into the device. With the intent to provide complete control to the power system under all types of potential malfunctions, fault-sensing circuitry has been included to sense over-voltage, under-voltage, or over-current conditions. Additionally, high-speed, pulse-by-pulse digital current limiting is included as a separate function. The operation of these circuits is described below.

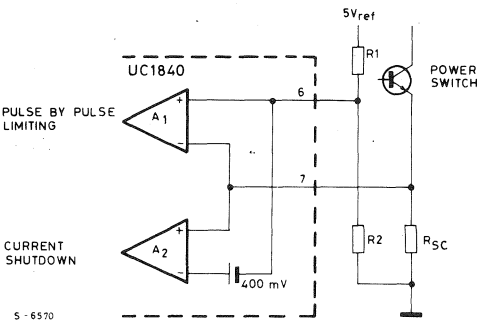
Fig. 14 - Interfacing the UC1840 single PWM output to a two-transistor off-line forward converter which uses proportional base drive.



Current limiting

The current limit comparators have differential inputs for noise rejection but are intended to be used with ground-referenced current sensing as in Figure 15. Comparator A1 is delegated to pulse-by-pulse current limiting. The output of this comparator drives the PWM comparator, where it activates the PWM latch, terminating each pulse when the current sensed by R_{SC} reaches a threshold defined by divider R1, R2, and the 5V reference.

Fig. 15 - Current limiting and overcurrent shutdown are implemented with comparators of different thresholds and a single current sense resistor.



Since V_C is intended to track the supply's output voltage, the addition of a resistor from pin 6 to V_C will provide some foldback to the current limit characteristic. Since comparator A1 has zero offset voltage, it is activated when the voltage across R_{SC} equals that across R2. Comparator A2, with an offset voltage of 400 mV, will activate for over-current shutdown when the voltage across R_{SC} rises to 400 mV higher than the voltage across R2. Since the input bias to both comparators is less than 5 μA, a low-pass filter for noise rejection may be inserted between R_{SC} and the sense inputs. Activation of comparator A2 is defined as an over-current fault and it triggers the Error Latch. Its operation follows.

Fault sequencing

The fault sequencing logic of the UC1840 is shown in Figure 16. Since a fault is defined by this device as an activation of the Error Latch, it makes sense to start here in an attempt to understand this portion of the circuitry. Setting the Error Latch immediately turns on Q1 and Q2, discharging the slow-start capacitor and terminating the PWM output. Note that there is an additional path from the inverted output of the Start/UV comparator through OR2 which keeps pin 8 low. This is to keep the slow-start low during initial turn-on which is not intended to be classified as a fault.

The input to the Error Latch is from OR1 which triggers on signals resulting from four possible events:

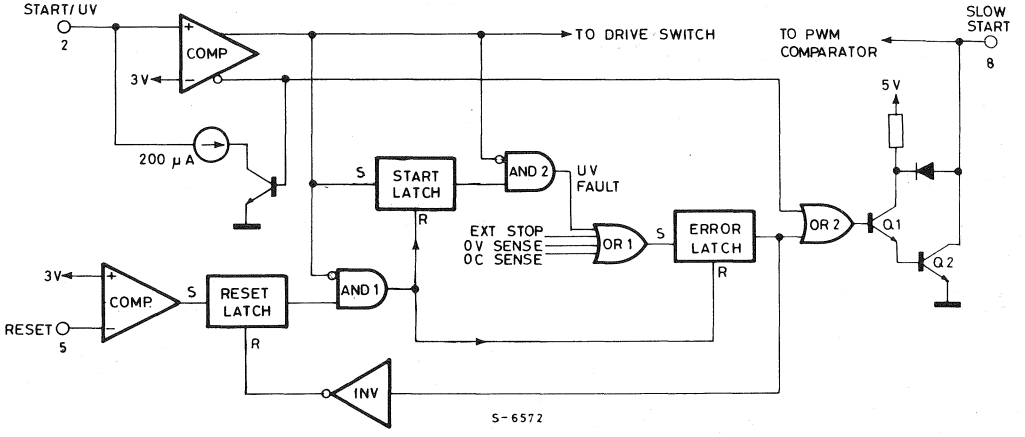
(1) A voltage less than 3V (after prior turn-on) at the Start/UV sense terminal, pin 2.

(2) A voltage greater than 3V at the Over-Voltage Sense terminal, pin 3.

(3) A voltage of less than 3V on the Ext. Stop terminal, pin 4.

(4) An over-current signal resulting in a differential voltage between pins 7 and 6 of greater than 400 mV.

Fig. 16 - Fault sequence logic is designed to insure a complete shutdown and fully controlled restart upon any of four possible fault conditions.



Any of these inputs need only be momentary to set the Error Latch. Transient protection may be necessary to eliminate false triggering, but it can be readily accomplished as all the comparator inputs are high impedances requiring less than 2 μA of input current, and the 3.0V reference yields a high noise immunity.

The Start Latch can be understood by recognizing that at initial turn-on it is reset with a low output. This prevents AND2 from transmitting a UV fault signal from the Start/UV non-inverting output to the Error Latch. At the start voltage level, defined by a high level on the Start/UV non-inverting output, the Start Latch sets but AND2 still provides no output. Only when the Start/UV input goes low again, with the Start Latch output held high, will AND2 yield an output into the Error Latch.

The status of the Reset terminal, pin 5, determines what happens after the Error Latch is set. The choices are:

(1) Latch off and require a recycle of input voltage to restart.

(2) Continuously attempt to restart.

(3) Attempt some number of restarts and then latch off.

(4) Latch off and await a momentary reset pulse to restart.

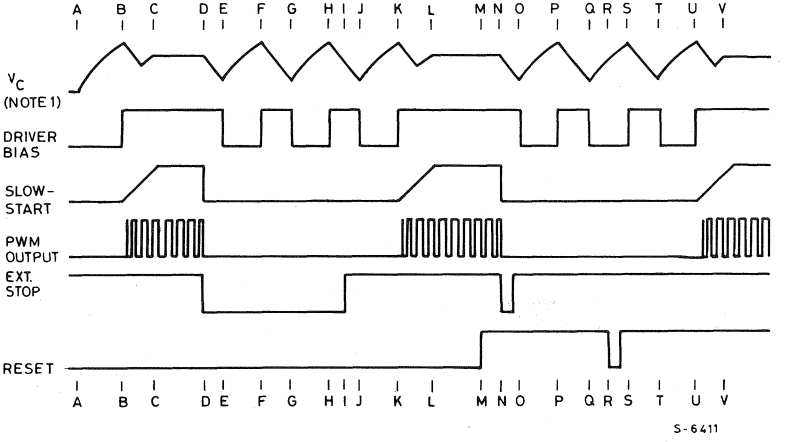
To examine the operation of the Reset Latch, note that prior to setting the Error Latch, its low output is inverted to hold the reset input to the Reset Latch high. This forces the Reset Latch's output low, regardless of the voltage on pin 5, and, thus, insures no signal out of AND1. With the setting of the Error Latch, the Reset Latch is free to take the

state commanded by pin 5: high if pin 5 is low and vice-versa. The latch allows merely a pulse to set the Reset Latch; the voltage on pin 5 need not be steady state.

With a high Reset Latch output, the Error Latch still does not reset until a low signal is sensed on the Start/UV sense terminal. At that point, AND1 then resets both the Error Latch and the Start Latch re-establishing the initial conditions for a normal start after fully charging the input capacitor. Of course, if the fault is still present, when the Start/UV input reaches the start level terminating the Error Latch reset signal, this latch will immediately set again.

To aid in the understanding of this logic, Figure 17 gives a pictorial representation of its operation with both steady-state and momentary signals on both the Ext. Stop and Reset terminals.

Fig. 17 - The interrelationship between the functions controlled by the fault sequence logic is illustrated with both static and pulse commands on the ext. stop and reset terminals.



Note 1: V_C represents an analog of the supply output voltage generated by a primary - referenced secondary winding on the power trasformer. It is the voltage monitored by the start/UV comparator and in most cases is the supply voltage V_{IN} for the UC1840.

TIME	EVENT
A	INITIAL TURN-ON V_C RISES WITH LIGHT LOAD.
B	START THRESHOLD DRIVER BIAS LOADS V_C.
C	OPERATING PWM REGULATES V_C.
D	STOP INPUT SETS. ERROR LATCH TURNING OFF PWM.
E	UV LOW THRESHOLD. ERROR LATCH REMAINS SET.
F	START TURNS ON DRIVER BIAS BUT ERROR LATCH STILL SET.
G	V_C AND DRIVER BIAS CONTINUE TO CYCLE.
H	
I	STOP COMMAND REMOVED.
J	ERROR LATCH RESET AT UV LOW THRESHOLD.
K	START THRESHOLD NOW REMOVES SLOW-START CLAMP.
L	RETURN TO NORMAL RUN STATE.
M	RESET LATCH SET SIGNAL REMOVED.
N	ERROR LATCH SET WITH MOMENTARY FAULT.
O	ERROR LATCH DOES NOT RESET AS RESET LATCH IS RESET.
P	V_C AND DRIVER BIAS RECYCLE WITH NO TURN-ON.
Q	
R	RESET LATCH IS SET WITH MOMENTARY RESET SIGNAL.
S	V_C MUST COMPLETE CYCLE TO TURN ON.
T	START AND ERROR LATCHES RESET.
U	NORMAL START INITIATED.
V	RETURN TO NORMAL RUN STATE.

If Driver Bias turn–on is used to pump an increment of charge into an integrating capacitor, and that capacitor voltage is applied to the Reset Terminal, some number of retrys could be programmed to take place before the Reset voltage rises to 3V, which would then lock the output OFF. Since Driver Bias continues to cycle in the latched–off state, the Reset terminal will remain high until it is either remotely pulled low or the input voltage to the controller is interrupted.

Note that an important element in any restart after a shutdown is the lowering of the voltage at the Start/UV terminal below its UV threshold. While this will occur normally in bootstrap–driven applications, this device can also be used with a constant driving voltage by externally applying a momentary pull–down signal to the Start/UV input after a fault shutdown.

CONCLUSION

With the UC1840, power supply designers now have a device specifically developed for off–line, primary control and one which has addressed the problems of operation under less than "ideal" or normal conditions. Not only does this device make it easier to comply with stringent isolation requirements by requiring a minimum of communication between primary and secondary, but it is also ideally suited for powering systems in remote locations where only a simple transmitted pulse is available for power sequencing.